Attorney's Docket No.: 07977-105001 / US3189

REMARKS

Reconsideration and allowance of the above-referenced application are respectfully requested.

The drawings stand objected to as not showing certain subject matter of certain enumerated claims. In response, claims 2, 10, 27, 32, and 37 have been cancelled herein. Claims 17 and 21-25 are amended to delete the driver TFTs as shown in the attached.

The objection to claims 2, 10, 27, 32, 37, and 51 has been obviated by the cancellation of claims 2, 10, 27, 32, and 37. Claim 51 further stands objected to based on the direction of the array of TFTs not being parallel or vertical to a side edge of the first substrate or cut side edges of the substrate. The Office Action explains that it is not clear which side edge applicant considers to be the side edge that is parallel or vertical to a direction of array of the TFTs. This contention is respectfully traversed, since the terms "parallel or vertical" is not defined in claim 51.

Claims 17 and 21-25 stand objected to as allegedly being incomplete for only reciting one side edge. In response, this language has been removed. The other objected-to language in these claims has also been removed herein by amendment.

Claims 61-64 as amended recite a non-conductive material or weakly conductive material that is applied to a side edge of a

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substrate, and a part of the bus line located adjacent to that side edge of the substrate. A pixel TFT is provided over the substrate. This is suitable for preventing static charge from being generated in the side edge of the substrate and in the part of the bus line located adjacent to the side edge of the substrate. For these reasons, it is respectfully suggested that this system is suitable for protecting the gate insulating film of the pixel TFT from static charge. This makes it quite useful in a thin gate insulating film. These claims have been amended to recite a gate insulating film having a thickness between 500-2000Å. This emphasizes the patentable distinctions, and thus renders these claims allowable.

Claims 2, 4, 6, 10, 13, 14, 17, 21-25, 27, 30-32, 35-37,40-42, 44, and 51-56 stand rejected under 35 U.S.C. 103(a) based on Japanese document JP 404 192 446A. This contention is respectfully traversed, and it is respectfully suggested that the rejection does not meet the Patent Office's burden of providing a *prima facie* of unpatentability. Page 6 of the Official Action alleges that the Japanese document teaches simultaneously attaining high heat conductivity with low stress, by sealing a semiconductor chip with thermosetting resin formed of a mixture of alumina and fused silica. However, it is respectfully suggested that the document does not suggest that the thermosetting resin seals over a liquid crystal material.

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In order to distinguish the present invention over the Japanese documents, independently claims 17 and 21-25 have been amended to recite a sealing material that seals a liquid crystal material. Because this sealing material seals the liquid crystal material, and a control circuit that comprises a control circuit chip is provided under and in contact with the sealing material, this system may miniaturize the final liquid crystal display.

The amendments to the claims are respectfully suggested to obviate the double patenting rejection.

In view of the above amendments and remarks, therefore, all of the claims should be in condition for allowance. A formal notice to that effect is respectfully solicited.

Please apply any charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: 11/4/08

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VERSION TO SHOW CHANGES MADE

In the Claims:

Claims 2, 10, 27, 32 and 37 have been cancelled.

The following claims have been amended as follows.

17. (Amended) An active matrix liquid crystal display comprising:

a plurality of pixel TFTs arranged in rows and columns over a first substrate and arrayed in a matrix;

[driver TFTs formed over said first substrate and forming a driver circuit for driving said pixel TFTs;

a bus line provided over said first substrate and connected with at least one of said pixel TFTs;]

a counter substrate located opposite to said first substrate;

a layer of a liquid crystal material provided between said first substrate and said counter substrate;

[a nonconductive or weakly conductive material applied or adhesively bonded to a side edge of said counter substrate and a side edge of said first substrate;]

a sealing material sealing said liquid crystal material and provided between said first substrate and said counter substrate [and inside said side edge of said counter substrate and said side edge of said first substrate]; and

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a control circuit comprising a [semiconductor] control circuit chip provided under and in contact with said sealing material [for controlling said driver circuit], said control circuit provided over said first substrate.

21. (Amended) An active matrix liquid crystal display comprising:

a plurality of pixel TFTs arranged in rows and columns over a first substrate and arrayed in a matrix;

[driver TFTs formed over said first substrate and forming a driver circuit for driving said pixel TFTs;]

a bus line provided over said first substrate and connected with at least one of said pixel TFTs;

a counter substrate located opposite to said first substrate;

a layer of a liquid crystal material provided between said first substrate and said counter substrate;

[a nonconductive or weakly conductive material applied or adhesively bonded to a side edge of said counter substrate and a side edge of said first substrate;]

a sealing material sealing said liquid crystal material and provided between said first substrate and said counter substrate [and inside said side edge of said counter substrate and said side edge of said first substrate]; and

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a control circuit comprising a [semiconductor] control circuit chip provided under and in contact with said sealing material [for controlling said driver circuit], said control circuit provided over said first substrate.

22. (Amended) An active matrix liquid crystal display comprising:

a plurality of pixel TFTs arranged in rows and columns over a first substrate and arrayed in a matrix;

[driver TFTs formed over said first substrate and forming a driver circuit for driving said pixel TFTs;

a bus line provided over said first substrate and connected with at least one of said pixel TFTs;]

a counter substrate located opposite to said first substrate;

a layer of a liquid crystal material provided between said first substrate and said counter substrate;

[a nonconductive or weakly conductive material applied or adhesively bonded to a side edge of said counter substrate and a side edge of said first substrate;]

a sealing material sealing said liquid crystal material and provided between said first substrate and said counter substrate [and inside said side edge of said counter substrate and said

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side edge of said first substrate], said sealing material being provided outside at least said pixel TFTs; and

a control circuit comprising a [semiconductor] control circuit chip provided under and in contact with said sealing material [for controlling said driver circuit], said control circuit provided over said first substrate.

23. (Amended) An active matrix liquid crystal display comprising:

a plurality of pixel TFTs arranged in rows and columns over a first substrate and arrayed in a matrix;

[driver TFTs formed over said first substrate and forming a driver circuit for driving said pixel TFTs;]

a bus line provided over said first substrate and connected with at least one of said pixel TFTs;

a counter substrate located opposite to said first substrate;

a layer of a liquid crystal material provided between said first substrate and said counter substrate;

[a nonconductive or weakly conductive material applied or adhesively bonded to a side edge of said counter substrate and a side edge of said first substrate;]

a sealing material sealing said liquid crystal material and provided between said first substrate and said counter substrate

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[and inside said side edge of said counter substrate and said side edge of said first substrate], said sealing material being provided outside at least said pixel TFTs [and said driver TFTs]; and

a control circuit comprising a [semiconductor] control circuit chip provided under and in contact with said sealing material [for controlling said driver circuit], said control circuit provided over said first substrate.

24. (Amended) A method of fabricating an active matrix liquid crystal display comprising:

a plurality of pixel TFTs arranged in rows and columns over a first substrate and arrayed in a matrix;

[driver TFTs formed over said first substrate and forming a driver circuit for driving said pixel TFTs;]

a bus line provided over said first substrate and connected with at least one of said pixel TFTs;

a counter substrate located opposite to said first substrate;

a layer of a liquid crystal material provided between said first substrate and said counter substrate;

a sealing material sealing said liquid crystal material and provided between said first substrate and said counter substrate and outside at least said pixel TFTs; and

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a control circuit comprising a [semiconductor] control circuit chip provided under and in contact with said sealing material [for controlling said driver circuit], said control circuit provided over said first substrate,

said method comprising

cutting said first substrate and said counter substrate [at a cut side edge of said first substrate and at a cut side edge of said counter substrate] outside said sealing material having said control circuit under and in contact with said sealing material[; and

applying or adhesively bonding a nonconductive or weakly conductive material to the cut side edge of said first substrate and the cut side edge of said counter substrate].

25. (Amended) A method of fabricating an active matrix liquid crystal display comprising:

a plurality of pixel TFTs arranged in rows and columns over a first substrate and arrayed in a matrix;

[driver TFTs formed over said first substrate and forming a driver circuit for driving said pixel TFTs;]

a bus line provided over said first substrate and connected with at least one of said pixel TFTs;

a counter substrate located opposite to said first substrate;

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a layer of a liquid crystal material provided between said first substrate and said counter substrate;

a sealing material sealing said liquid crystal material and provided between said first substrate and said counter substrate [and outside said pixel TFTs and said driver TFTs]; and

a control circuit comprising a [semiconductor] control circuit chip provided under and in contact with said sealing material [for controlling said driver circuit], said control circuit provided over said first substrate,

said method comprising:

cutting said first substrate and said counter substrate [at a cut side edge of said first substrate and at a cut side edge of said counter substrate] outside said sealing material having said control circuit under and in contact with said sealing material[; and

applying or adhesively bonding a nonconductive or weakly conductive material to the cut side edge of said first substrate and the cut side edge of said counter substrate].

61. (Amended) A semiconductor device comprising:

a pixel TFT provided over a first substrate comprising a glass;

a channel formation region provided in a semiconductor film provided over said first substrate;

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a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween, said pixel TFT comprising said channel formation region and said gate electrode and said gate insulating film;

a counter substrate located opposite to said first substrate;

a bus line provided over said first substrate and connected with said pixel TFT, said bus line having a part located adjacent to a side edge of said first substrate;

a sealing material provided between said first substrate and said counter substrate; and

a nonconductive material applied to a side edge of said counter substrate and said side edge of said first substrate and said part of said bus line,

wherein said nonconductive material is provided on an outer side of said sealing material, and

wherein said gate insulating film has a thickness of 500 to 2000 Å.

62. (Amended) A semiconductor device comprising:

a pixel TFT provided over a first substrate comprising a glass;

a channel formation region provided in a semiconductor film provided over said first substrate;

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a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween, said pixel TFT comprising said channel formation region and said gate electrode and said gate insulating film;

a counter substrate located opposite to said first substrate;

a bus line provided over said first substrate and connected with said pixel TFT, said bus line having a part located adjacent to a side edge of said first substrate;

a sealing material provided between said first substrate and said counter substrate; and

a weakly conductive material applied to a side edge of said counter substrate and said side edge of said first substrate and said part of said bus line,

wherein said weakly conductive material is provided on an outer side of said sealing material, and

wherein said gate insulating film has a thickness of 500 to 2000 Å.

63. (Amended) A semiconductor device comprising:

a pixel TFT provided over a first substrate comprising a glass;

a channel formation region provided in a semiconductor film provided over said first substrate;

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a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween, said pixel TFT comprising said channel formation region and said gate electrode and said gate insulating film;

a driver TFT provided over said first substrate;

a counter substrate located opposite to said first substrate;

a bus line provided over said first substrate and connected with said pixel TFT, said bus line having a part located adjacent to a side edge of said first substrate;

a sealing material provided between said first substrate and said counter substrate; and

a nonconductive material applied to a side edge of said counter substrate and said side edge of said first substrate and said part of said bus line,

wherein said nonconductive material is provided on an outer side of said sealing material, and

wherein said gate insulating film has a thickness of 500 to 2000 Å.

64. (Amended) A semiconductor device comprising:

a pixel TFT provided over a first substrate comprising a glass;

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a channel formation region provided in a semiconductor film provided over said first substrate;

a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween, said pixel TFT comprising said channel formation region and said gate electrode and said gate insulating film;

a driver TFT provided over said first substrate;

a counter substrate located opposite to said first substrate;

a bus line provided over said first substrate and connected with said pixel TFT, said bus line having a part located adjacent to a side edge of said first substrate;

a sealing material provided between said first substrate and said counter substrate; and

a weakly conductive material applied to a side edge of said counter substrate and said side edge of said first substrate and said part of said bus line,

wherein said weakly conductive material is provided on an outer side of said sealing material, and

wherein said gate insulating film has a thickness of 500 to 2000 Å.

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